**Charge-integrating organic heterojunction phototransistors for wide-dynamic-range image sensors**

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Supplementary Figure 1. Transfer characteristic of the organic phototransistor showing the close fit to square-law behavior and small hysteresis.

Supplementary Figure 2. Histograms showing the distribution of saturation mobility, on-off ratio, and threshold voltage for 40 organic phototransistors.
Supplementary Figure 3. a, Water contact angle on PCDTBT:PC$_{71}$BM. b, Atomic force microscopy (AFM) images of DNTT on PCDTBT:PC$_{71}$BM. c, AFM images of PCDTBT:PC$_{71}$BM.

Supplementary Figure 4. EQE of an organic photodiode (OPD) composed of 1:3 PCDTBT:PC$_{71}$BM by weight of the same active layer thickness (45 nm) as the same BHJ absorbing layer in the phototransistor. The active layer is sandwiched between a PEDOT:PSS anode and an aluminum cathode.

Supplementary Figure 5. Transfer characteristics of the phototransistor under dark and an irradiance of 40 μW/cm$^2$ at 532 nm.

The biasing capacitor $C_B$ compensates for the change of charge in the source electrode resulting from parasitic source-gate capacitance $C_{GS}$ when the device is switched to integration mode as explained in Supplementary Fig. 6. The source electrode is set to 0 V when the phototransistor is on since the drain is connected to virtual ground, resulting in an accumulated parasitic charge of 15.4 pC for a $V_{GS}$ of -14 V and $C_{GS}$ of 1.1 pF. Turning off the device results in a transfer of $(V_{on}-V_{off})C_{GS} = 22$ pC to $C_B$ assuming no charge dissipation from the source electrode through the
channel when turning off the device. This charge transfer biases $V_{DS}$ at -5.37 V during integration, and is independent of the applied bias voltage, $V_B$.

Supplementary Figure 6. $V_{SD}$ in off-state

Supplementary Figure 7. The amount of integrated charge readout from the pixel as a function of readout delay. This delay is defined as the time between the extinguishing of the light source and readout of the pixel. The light is illuminated at an irradiance of 40 $\mu$W/cm$^2$ at 532 nm for and integrated for 20 ms.

The dependence of illuminated region of the phototransistor-based pixel is examined using another pixel architecture as shown in Supplementary Fig. 8a. The equivalent circuit diagram and highlighted regions of the pixel in Supplementary Fig. 8a are shown in Supplementary Fig. 8b. The optoelectronic performance of each region is assessed by individually illuminating the channel (blue), drain-gate $C_{GD}$ overlap (green), and bias capacitor $C_B$ (black) and looking at the discharge characteristics. Supplementary Fig. 8c plots these results. The discharge from only illuminating the channel (blue) displays a transient behavior as a result of the transit time of carriers through the channel. However, the discharge of only illuminating $C_{GD}$ does not exhibit a transient response since carriers are transferred directly between the active layer to the underlying drain electrode without having to go through a resistive channel. No photoresponse is seen from only illuminating $C_B$ since the one-to-one ratio of photogenerated electrons to holes maintains charge neutrality in the source electrode and does not change biasing. Given these results, the photoactive area for phototransistors is considered to be the channel and overlapping gate-drain electrodes.
Supplementary Figure 8: Photosensitive regions of a test phototransistor structure highlighted in the optical micrograph a and equivalent circuit b. c. Transient discharge plot for various illuminated regions in the phototransistor test pixel.

A conventional charge-integrating photodiode-based pixel architecture, comprised of a photodiode in series with a transistor$^{8, 22, 24}$, is fabricated from the same material set as the phototransistor in order to compare the performance of photodiode and phototransistor-based pixel architectures. The pixel schematic and driving-readout scheme are shown in Supplementary Fig. 9a and b, respectively. The cross section of the pixel, depicting the photodiode and transistor areas, and equivalent circuit are shown in Supplementary Fig. 9c and d, respectively. The TFT has the same channel architecture and the phototransistor but is covered in order to render it unresponsive to light. Dynamic responses of phototransistor- and photodiode-based pixel are compared in Supplementary Fig. 9e across a wide range of irradiances at 532 nm. At a sampling rate of 30 fps, the photodiode-based pixel has a dynamic range of 64 dB, which is comparable to the 70 dB of consumer-grade CMOS sensors$^{21}$. The dynamic range of the photodiode-based architecture is limited by the well capacity of the photodiode, resulting in a distinct plateau of the responsivity of this pixel at high irradiances while the phototransistor-based pixel continues to give an irradiance-dependent response. Supplementary Fig. 9f shows the photodiode-based pixel is limited to the EQE of the photodiode at low irradiances, which is 63% according to Supplementary Fig. 4. The phototransistor pixel is also more efficient than the photodiode pixel across its dynamic range, which ends at the saturation of the photodiode’s well capacity.
Supplementary Figure 9: Photodiode pixel architecture, operation, and performance. a, Schematic view of photodiode-based pixel. b, Driving and readout scheme of the pixel. c, Cross-sectional view of the pixel. d, Equivalent circuit. e, Output integrated charge from the pixel versus irradiance at 532 nm in comparison to an organic phototransistor (OPT)-based pixel. The Photodiode pixel saturates at approximately 40 μW/cm², error bars represent the standard deviation of the signal. f, External quantum efficiency of the integrated signal (EQEint) of plot e.

Supplementary Figure 10. Normalized lag of the imaged irradiance after a light source of 28 μW/cm² at 532 nm is extinguished at the time of the first data point. Each data point represents the readout charge from a pixel at a rate of 30 fps.

Supplementary Fig. 11 illustrates the process flow for fabricating an array of discrete phototransistor-based pixels. Supplementary Fig. 12 shows the stainless steel stencil design used to pattern the surface energy of the substrate during plasma treatment. After surface treatment, the ink is uniformly dispensed across an ink reservoir (1) located at the top of the pattern before using a doctor blade...
positioned 100 μm above the substrate to drag the ink across (2). The bias capacitor and readout row lines from the drain are then screen printed, followed by a dielectric separator and the gate column lines.

Supplementary Figure 11: Phototransistor pixel fabrication process flow as explained in the methods section.

Supplementary Fig. 13 shows the I/O circuitry used to drive and readout the phototransistor-based pixel. An Analog Discovery digital oscilloscope and function generator from Digilent is used to generate the waveforms needed for the pixel. Inverting amplifiers are used to amplify the voltage to the bias capacitor and gate of the pixel. A charge amplifier is placed at the output of the pixel in order to
determine the amount of charge output from the pixel and is readout from the oscilloscope channel on the Analog Discovery.

Supplementary Figure 13: I/O drivers for phototransistor-based pixel.