Supplementary Information

Section S1. Device fabrication process

Railed microfluidic devices fabrication

Railed microfluidic channels were prepared using standard photolithography and soft lithography methods. A two-layer microfluidic channel with a groove structure was fabricated using a two-layer mold fabrication process by repeating photolithography twice in the mold preparation phase (Fig. S1). For the photolithography process, SU-8 2015 photoresist (Microchem) was first spin-coated on a silicon wafer at 1000 rpm velocity for 30 seconds (approximately 40 μm of SU-8 photoresist thickness) (Fig. S1 (a)). It was then baked for 5 minutes at 95°C on a hotplate. Second, channel layer was patterned through a film photomask (designed by AUTOCAD) of 25,000 dpi resolution and baked for 6 minutes at 95°C on a hotplate. The patterned wafer was then developed for 10 minutes in SU-8 developer (Fig. S1 (b)). Third, additional SU-8 photoresist was spin-coated on the top of the channel layer (Fig. S1 (c)), and then rail-layer was patterned (Fig. S1 (d)). Finally, hard bake of the patterned wafer was performed for 10 minutes at 110°C on a hotplate, then two-layer patterned silicon wafer mold was prepared. For soft-lithography process, the mold was transferred to Polydimethylsiloxane (PDMS) Silicon 1 Elastomer (Sylgard 184, Dow Corning) material with 10 wt% of curing agent by baking 10 minutes on a hotplate of 150°C (Fig. S1 (e)). Then the replica PDMS mold was bonded onto the PDMS-coated slide glass through 20 seconds of plasma cleaning process under 500~1000 mbar vacuum condition with Plasma Cleaner PDC-32G (Harrick Plasma) to complete the railed microfluidic channel
fabrication process (Fig. S1 (f)). The channels were punched at each inlet and outlet, and connected to pipette tips with silicon tubing to a syringe pump (KD Scientific).

Figure S1. Fabrication process of a two-layer microfluidic channel with a guiding rail structure (a) Photoresist (SU-8) coating on a silicon wafer (b) Channel layer patterning (c) Additional photoresist coating on top of the channel layer (d) Rail-layer patterning (e) Transferring the two-layer patterns to PDMS material (f) Bonding the replica PDMS mold onto the PDMS-coated slide glass

**Silicon microchips fabrication**

Silicon microchips have 100µm × 100µm dimension with 20µm thickness. To fabricate these microchips, a 4 inch-sized SOI (Silicon On Insulator) wafer with a 20-µm-thick device layer was cleaned with 4:1 (vol/vol) H₂SO₄/H₂O₂ solution for 360 seconds (Fig. S2 (a)). Cleaned SOI wafer was spin-coated with HMDS for 7 seconds at 2500rpm velocity to enhance the adhesion of AZ1512 photoresist. After HMDS coating, AZ1512 positive photoresist was spin-coated for 40 seconds at 4000rpm velocity. It was then baked for 90
seconds at 88°C on a hotplate (soft bake). After 20 seconds of UV exposure through a film photomask of 25,000 dpi resolution, the wafer was baked for 60 seconds at 110°C on a hotplate (post exposure bake). In addition, 3 minutes develop in AZ300MIF developer is processed, and then baked for 10 minutes at 110°C on a hotplate (hard bake) (Fig. S2 (b)).

We used this patterned AZ1512 on a SOI wafer as an etch mask for deep reactive ion etch (Deep Si Etcher, Plasma Therm) through the device layer down to the buried oxide (20µm) (Fig. S2 (c)). We then removed the remnant photoresist with Asher (Plasma Finish) for 600 seconds (Fig. S2 (d)). After final cleaning with 4:1 (vol/vol) H₂SO₄/H₂O₂ solution for 5 minutes, we released silicon microchips by immersing the wafer in a 49% hydrofluoric acid for 3 hours (Fig. S2 (e)). By filtering released microchips with filter paper and cleaning with deionized (D.I.) water, we collected 100µm x 100µm sized silicon microchips in D. I. water (Fig. S2 (f)). For the experiments, silicon chips were dispersed in poly (ethylene glycol) diacrylate (PEG-DA, Sigma-Aldrich, Mₙ=258) with 5 wt% of photoinitiator (2, 2-dimethoxy-2-phenylacetophenone).
Figure S2. Fabrication process of silicon microchips (a) Preparing cleaned SOI wafer, (b) Microchip patterning as an etch mask, (c) Deep reactive ion etch, (d) Photoresist strip and SPM cleaning, (e) Microchip release in 49% hydrofluoric acid, (f) Collecting diluted silicon chips in D.I. water. Scale bars are 100µm.
Section S2. Design of the rail

One of the details requiring attention for successful railed transports is the depth of the rail. During the polymerization process, the PDMS channel surface is inhibited due to the high oxygen concentration near the channel wall. The height of a fabricated microtrain is slightly smaller than the channel height, as shown in Fig. S3(a). Details about this oxygen inhibition layer have been previously discussed\textsuperscript{1,2}. The oxygen inhibition layer is a space where UV curable solution is not photopolymerized, allowing for fabricated microtrains to move upward or downward flexibly. Therefore microtrains can be derailed if the depth of rail is too shallow, as shown in Fig. S3(b). To prevent the derailing of the microtrains, the depth of the rail (d\textsubscript{r}) should be larger than at least twice the depth of the inhibition layer (d\textsubscript{i}) (Fig. S3(a)). Considering that the microtrain and channel are relatively flexible polymeric structures, the depth of the rail should have more room than the critical number of two times the thickness of the inhibition layer. In the microfluidic channel, the thickness of the oxygen inhibition layer ranges from 3-5\textmu m for both the top and bottom layers in the 40\textmu m-height microfluidic channel. Therefore, the actual rail depth we used in the experiments is 15\textmu m, in consideration of the flexible polymeric structures.
Figure S3. Design rule for the depth of the rail

(a) The depth of the rail is deeper than two times the oxygen inhibition layer’s thickness ($d_r > 2d_i$), (b) The depth of the rail is smaller than two times the oxygen inhibition layer’s thickness ($d_r < 2d_i$)

Section S3. Guided self-assembly in railed microfluidics

Sequential steps of 2D self-assembly of microlatches

By repeating the assembly process of two-dimensional self-assembly described in the paper, multiple chains of microlatches were stacked to form a 5 x 5 matrix of microlatches. Fig. S4 (a)-(d) show sequential steps of 2D microlatch array. This process is scalable to large area assembly.
Figure S4. Sequential steps of 2D assembly in forming 5 x 5 matrix. (a) 2-layer assembly (b) 3-layer assembly (c) 4-layer assembly (d) 5-layer assembly.

**Experimental process of complex self-assembly**

The real benefit of railed microfluidics over the conventional fluidic self-assembly lies in its capability to assemble complex systems made up of a large number of different parts. Here, all microstructures are assembled together at the end of rails. The complex self-assembled system is completed simultaneously by applying fluidic force inside a railed microfluidic channel. Fig. S5 shows the experimental process of complex self-assembly using railed microfluidic channels.
First, we prepare railed microfluidic channel fabricated by the process presented in Supplementary Information S1 (Microfluidic device fabrication) and introduce UV curable solution into a railed microfluidic channel (Fig. S5 (a)). The flow rate of the solution is controlled by a syringe pump. Each microtrain is fabricated independently on a corresponding rail via optofluidic maskless lithography (Fig. S5(b)). Fig. S5 (d)-(e) show the fabrication of two different shapes, striped circle-shape microtrain and cross-shape microtrain. All the microstructures are assembled together at the end of the rails (Fig. S5(c)). Fig. S5 (f) shows the assembled complex structure.

Figure S5. Experimental process of complex self-assembly (a) Introduce UV curable solution into a railed microfluidic channel. (b) Fabrication of each microtrain independently on a corresponding rail via optofluidic maskless lithography. (c) All the microtrains are assembled
at the end of the rails (d)-(f) Process of fabrication and assembly. Microtrains are fabricated on corresponding rails (d)-(e), and self-assembled at the end of the rails (f).

Fig. S6 shows another fabrication example of Greek temple shown in Fig. 3(a). Each microstructure is fabricated independently on a corresponding rail (Fig. S6(a)-(d)). Then, all the microstructures are assembled together at the end of rails by applying fluidic force (Fig. S6(e)).

Figure S6. Fabrication process of Greek temple assembly (a)-(d) Each microtrain is fabricated independently on a corresponding rail. (a) Support (b) Pillar (c) Roof support (d) Roof (e) All microtrains are assembled together at the end of the rails. The complex self-assembled system is completed simultaneously by applying fluidic force inside a railed microfluidic channel.

Examples of other self-assembled complex systems

The self-assembled complex structures can be easily actuated like the crawling microcentipede assembly as shown in Fig. S7(a). After assembly of parts forming a whole microcentipede body, the assembled microcentipede system crawls when reverse fluidic force is applied (See Supplementary Information Movie S3).
In addition, there is a great variety of possible rail system designs. As shown in the assembly of a micro-zipper (Fig. S7 (b)), two curved rails could initiate the assembly process. If the length of the microstructures is longer than the bending radius of the bending rail, the bend works as a topological barrier, much like the end of the rail. The upper and lower zippers are fabricated on the upper and lower rails, respectively. Upon applying liquid flow, the two zippers get closer, are engaged at the bend, and finally are zipped together as they pass through the bend.

![Image](image.png)

Figure S7. Examples of other interesting complex self-assembled microsystems in railed microfluidics (a) Microcentipede. (b) Micro-zipper. Two zippers get closer, are engaged at the bend, and finally are “zipped” together when they pass through the bend.

References
