Synthesis of ultrathin polymer insulating layers by initiated chemical vapour deposition for low-power soft electronics

Hanul Moon†, Hyejeong Seong†, Woo Cheol Shin†, Won-Tae Park, Mincheol Kim, Seungwon Lee, Jae Hoon Bong, Yong-Young Noh, Byung Jin Cho*, Seunghyup Yoo* & Sung Gap Im*
Leakage current density ($J$) vs. applied voltage ($V$) characteristics of initiated chemical vapor deposited (iCVD) polymer insulating layers from various monomers. $J$-$V$ curves of metal/insulator/metal (MIM) devices of Al(50 nm)/iCVD polymer insulator (various thicknesses)/Al(50 nm) structure, with various iCVD polymer layers: a) poly(ethylene glycol dimethacrylate) (pEGDMA), b) poly(isobonyl acrylate) (pIBA), c) poly(1-vinylimidazole) (pVIDZ), d) poly(1H,1H,2H,2H-perfluorodecyl acrylate) (pPFDA), e) poly(1,3,5-trimethyl-1,3,5-trivinyl cyclotrisiloxane) (pV3D3), and f) random copolymer of PFDA-V3D3 of 1:1. The polymerization schemes and the thicknesses of the iCVD polymer films are denoted on the corresponding $J$-$V$ curves. For some polymer layers, capacitance density ($C$) vs. $V$ plots are depicted in inset of the graphs.

In all the iCVD polymerization process, tert-butyl peroxide (TBPO) is commonly used as an initiator. The tested iCVD polymer insulators of 5 homopolymers and 1 random copolymer, show remarkably low leakage current. These observations clearly indicate that the iCVD process can produce a variety of uniform, defect-free polymeric insulator films.
**Figure S2.**

**Chemical structures of the pV3D3 layer.** a) Fourier transform infrared (FTIR) spectra of V3D3 monomer (gray) and iCVD pV3D3 polymer (blue). b) Survey scan of X-ray photoelectron spectrum (XPS), and c) X-ray diffraction (XRD) spectra of iCVD pV3D3 polymer films.

![FTIR spectra](image1)

![Survey scan XPS](image2)

![XRD spectra](image3)

**Table S1.**

<table>
<thead>
<tr>
<th>Atoms</th>
<th>Measured value [%]</th>
<th>Theoretical value [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>60.9</td>
<td>60</td>
</tr>
<tr>
<td>O</td>
<td>17.04</td>
<td>20</td>
</tr>
<tr>
<td>Si</td>
<td>22.06</td>
<td>20</td>
</tr>
<tr>
<td>Total</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

FTIR peak assignments associated with the V3D3 monomer and the corresponding polymer have been previously reported. Briefly, the C=C stretch peaks of vinyl bond and CH$_2$ deformation are present at 1410 cm$^{-1}$ and 1600 cm$^{-1}$, respectively in the V3D3 spectrum, disappeared in the pV3D3 spectrum, confirming that the vinyl moieties present in the monomers are converted to aliphatic sp$^3$ bonding in the pV3D3 polymer films during the iCVD process.

A quantitative analysis of the elements in the XPS spectrum showed the atomic ratio of C:O:Si of near to 3:1:1, which is the theoretical atomic ratio of the pV3D3. Thus, the FTIR and XPS data clearly demonstrate that the pV3D3 is successfully formed via the iCVD process.

An XRD spectrum of pV3D3 layer shows no distinctive peaks, indicating that the iCVD pV3D3 films are amorphous, which is consistent with the transmission electron microscope (TEM) images of the MIM structures shown in Figure 1.

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Table S2.

Chemical resistance of the iCVD pV3D3 layer against various organic solvents. The thickness \(d_{pV3D3}\) and surface morphology of pV3D3 layers on Si wafers were measured before and after a 24-hr soak in various organic solvents.

<table>
<thead>
<tr>
<th>Solvent</th>
<th>(d_{pV3D3,AFM}) [nm](^a) before</th>
<th>(d_{pV3D3,AFM}) [nm] after</th>
<th>(R_q) [nm](^b) before</th>
<th>(R_q) [nm] after</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acetone</td>
<td>91.9</td>
<td>92.9</td>
<td>0.42</td>
<td>0.57</td>
</tr>
<tr>
<td>THF(^c)</td>
<td>63.2</td>
<td>61.1</td>
<td>0.42</td>
<td>0.39</td>
</tr>
<tr>
<td>Toluene</td>
<td>82.3</td>
<td>82.0</td>
<td>0.42</td>
<td>0.46</td>
</tr>
</tbody>
</table>

\(^a\) \(d_{pV3D3,AFM}\): pV3D3 layer thicknesses measured by atomic force microscopy (AFM)

\(^b\) \(R_q\): root-mean-square (RMS) surface roughness of pV3D3 layers

\(^c\) THF: tetrahydrofuran

Figure S3.

AFM images of the as-deposited pV3D3 layer and the layers after the 24-hr soak in acetone, THF, and toluene, respectively.

Both the \(d_{pV3D3}\) and the surface morphology of pV3D3 layers were virtually unchanged, confirming that pV3D3 layers are highly durable against various organic solvents.
Table S2. Chemical resistance of the iCVD pV3D3 layer against various organic solvents. The thickness (d_{pV3D3}) and surface morphology of pV3D3 layers on Si wafers were measured before and after a 24-hr soak in various organic solvents.

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<th>Solvent</th>
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b R_q: root-mean-square (RMS) surface roughness of pV3D3 layers
c THF: tetrahydrofuran

Figure S3. AFM images of the as-deposited pV3D3 layer and the layers after the 24-hr soak in acetone, THF, and toluene, respectively. Both the d_{pV3D3} and the surface morphology of pV3D3 layers were virtually unchanged, confirming that pV3D3 layers are highly durable against various organic solvents.

Figure S4. Thermal stability of the MIM devices with iCVD pV3D3 layers and Al electrodes. a) The change of J_i at an applied electric field (E_i) of 3 MV/cm with varying annealing times from 1 to 600 min with an annealing temperature of 250 and 350 °C. b) Thermogravimetric analysis (TGA) of pV3D3. All the annealing and measurements were performed in a N_2 atmosphere.

The thermal stability of the pV3D3 layers was investigated using MIM device configuration (Al/pV3D3/Al) in N_2 atmosphere, and the MIM device withstood the thermal stress of 250 °C for more than 8 hours. However, the pV3D3 layer became leaky with a 30-minute annealing at 350 °C, and that is well consistent with the thermogravimetric analysis (TGA) result of pV3D3, indicating a thermal degradation of pV3D3 starts to occur at 350 °C.
Figure S5.

**Estimation of the iCVD pV3D3 band energies.** a) Electron energy loss spectroscopy (EELS) spectra (left) of SiO$_2$ (gray) and pV3D3 (blue) and the enlarged EELS spectra of SiO$_2$ (middle) and pV3D3 (right). Ultraviolet photoelectron spectroscopy (UPS) spectra of b) Au and c) pV3D3. The enlarged UPS spectra at highest binding energy cut-off (middle) and lowest binding energy cut-off (right) are also shown for corresponding materials.

In many cases, the bandgap ($E_g$) of materials have been estimated by optical absorption spectrum, but for a dielectric layer with a large $E_g$ the detection limit of UV-visible spectrometry makes this optical method impractical. 3 In this study an EELS$^{4,5}$ analysis was performed to measure the wide $E_g$ of pV3D3 films. Figure S5a shows the EELS spectrum of a 100 nm-thick iCVD pV3D3 film. The spectrum of 100 nm-thick SiO$_2$ is also taken as a control. The $E_g$ value extracted from the linear fit of EELS spectrum is 8.25 eV for pV3D3, and it is also confirmed that the $E_g$ measured for the control SiO$_2$ (8.7 eV) matches closely with the reported value in the literature (9.0 eV). 6

UPS analysis was also performed to understand the electronic structure of the highest occupied molecular orbital (HOMO) level in pV3D3. For UPS, He I discharge at 21.22 eV was used and the Fermi edge ($E_F$) was calibrated with gold before the measurement. Figure S5b and c shows the UPS spectra of the Au layer deposited by thermal evaporation and the 100 nm-thick iCVD pV3D3 film, respectively. As shown in I and II in Figure S5b, the secondary electron cutoff ($E_{cutoff}$) and $E_F$ of Au

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Figure S5. Estimation of the iCVD pV3D3 band energies. (a) Electron energy loss spectroscopy (EELS) spectra (left) of SiO2 (gray) and pV3D3 (blue) and the enlarged EELS spectra of SiO2 (middle) and pV3D3 (right). Ultraviolet photoelectron spectroscopy (UPS) spectra of (b) Au and (c) pV3D3. The enlarged UPS spectra at highest binding energy cut-off (middle) and lowest binding energy cut-off (right) are also shown for corresponding materials.

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The secondary electron cutoff (\(E_{\text{cutoff}}\)) and the highest occupied molecular orbital (HOMO) level cutoff (\(E_{\text{HOMO,cutoff}}\)) of pV3D3 films were 16.42 eV and 4.2 eV, respectively, as shown in Figure S5c-I and II. Combining \(E_g\) of pV3D3 and \(E_F\) of Au, the complete band energy structure of pV3D3 was determined and shown in Figure 1c.
Figure S6.

Uniformity of MIM devices using pV3D3 insulating layers with Al electrodes. **a)** The position of 6 substrates during the pV3D3 deposition in an iCVD chamber and 6 MIMs of Al/pV3D3/Al under test for each substrate. **b)** The spatial distribution and **c)** the cumulative distribution of $C_i$ measured from 36 MIMs with 12.2±0.3 nm-thick pV3D3 layers over the area of 5×10 cm$^2$. **d)** The layout for test samples: two sample layouts of Type A and Type B, which are only slightly different from each other, were used in this work. In Type A, 20 MIMs within the red dashed line were tested out of 28 devices as the remaining devices near the edges were often subject to accidental scratches during sample handling; In Type B, all 16 MIMs were tested. **e)** The cumulative distribution of $C_i$ and $J_i$, and **f)** overlapped $J_i$-$E_i$ curves for pV3D3 thickness ($d_{pV3D3}$) of 12.5 nm, 6 nm and 7.8 nm. 20 MIMs were measured in one substrate for each 12.5 nm and 6 nm-thick pV3D3 layers that were fabricated in the same batch using the Type A device pattern, and 16 MIMs were measured in one substrate to test the 7.8 nm-thick pV3D3 layer that was fabricated using the Type B sample layout in a separate batch from the other two thicknesses. The size of MIMs is 1mm×1mm. In **f)**, 6 MIMs with $d_{pV3D3}$ of 6 nm were characterized in both forward and reverse biases while the remaining 12 MIMs with the same $d_{pV3D3}$ were characterized in only forward bias considering their symmetric characteristics.

<table>
<thead>
<tr>
<th>Dev. layout</th>
<th>Yield*</th>
<th>Average</th>
<th>Standard deviation</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>36 MIMs from 6 substrates</td>
<td>Type A</td>
<td>$C_i$ [nF/cm]</td>
<td>160</td>
<td>4</td>
<td>155</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$d_{pV3D3}$ [nm]</td>
<td>12.2</td>
<td>0.3</td>
<td>11.5</td>
</tr>
<tr>
<td>20 MIMs from 1 substrate</td>
<td>Type A</td>
<td>$C_i$ [nF/cm]</td>
<td>156</td>
<td>6</td>
<td>149</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$d_{pV3D3}$ [nm]</td>
<td>12.5</td>
<td>0.4</td>
<td>11.8</td>
</tr>
<tr>
<td>18 MIMs from 1 substrate</td>
<td>Type A</td>
<td>$C_i$ [nF/cm]</td>
<td>323</td>
<td>6</td>
<td>314</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$d_{pV3D3}$ [nm]</td>
<td>6.0</td>
<td>0.1</td>
<td>5.9</td>
</tr>
<tr>
<td>15 MIMs from 1 substrate</td>
<td>Type B</td>
<td>$C_i$ [nF/cm]</td>
<td>251</td>
<td>6</td>
<td>244</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$d_{pV3D3}$ [nm]</td>
<td>7.8</td>
<td>0.2</td>
<td>7.3</td>
</tr>
</tbody>
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* Yield was defined as the ratio of the number of MIM devices with $J_i$ (at $E_i=3$ MV/cm) on the order of ~10$^{-7}$ A/cm$^2$ or less to the number of all the MIM devices tested in a given substrate.
Figure S6. Uniformity of MIM devices using pV3D3 in insulating layers with Al electrodes. 

(a) The position of 6 substrates during the pV3D3 deposition in an iCVD chamber and 6 MIMs of Al/pV3D3/Al under test for each substrate. 

(b) The spatial distribution and 

c) the cumulative distribution of $C_i$ measured from 36 MIMs with 12.2±0.3 nm-thick pV3D3 layers over the area of 5×10$^2$ cm$^2$. 

d) The layout for test samples: two sample layouts of Type A and Type B, which are only slightly different from each other, were used in this work. In Type A, 20 MIMs within the red dashed line were tested out of 28 devices as the remaining devices near the edges were often subject to accidental scratches during sample handling; In Type B, all 16 MIMs were tested. 

e) The cumulative distribution of $C_i$ and 

f) overla$\bar{d}$ $J_i$ curves for pV3D3 thickness ($d_{pV3D3}$) of 12.5 nm, 6 nm and 7.8 nm. 20 MIMs were measured in one substrate for each 12.5 nm and 6 nm-thick pV3D3 layers that were fabricated in the same batch using the Type A device pattern, and 16 MIMs were measured in one substrate to test the 7.8 nm-thick pV3D3 layer that was fabricated using the Type B sample layout in a separate batch from the other two thicknesses. The size of MIMs is 1mm×1mm. * In f), 6 MIMs with $d_{pV3D3}$ of 6 nm were characterized in both forward and reverse biases while the remaining 12 MIMs with the same $d_{pV3D3}$ were characterized in only forward bias considering their symmetric characteristics. 

Table S3. 

<table>
<thead>
<tr>
<th>Dev. layout (Yield*)</th>
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</tr>
</thead>
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</tr>
<tr>
<td></td>
<td>-</td>
<td>$d_{pV3D3}$ [nm]</td>
<td>12.2</td>
<td>0.3</td>
</tr>
<tr>
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<td>6</td>
</tr>
<tr>
<td></td>
<td>20/20</td>
<td>$d_{pV3D3}$ [nm]</td>
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<td>0.4</td>
</tr>
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<td>$C_i$ [nF/cm]</td>
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</tr>
<tr>
<td></td>
<td>18/20</td>
<td>$d_{pV3D3}$ [nm]</td>
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<td>0.1</td>
</tr>
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Figure S7.

Insulating properties of the iCVD pV3D3 layers measured using metal/insulator/metal (MIM) devices with non-reactive electrodes.

**Part A. Characteristics of TaN/pV3D3/Au devices.**

- **a)** MIM device structure with a tantalum nitride (TaN)\(^7\) bottom electrode and an Au top electrode.
- **b)** The \(J_i-E_i\) and **c)** \(C_i-V_i\) characteristics with \(d_{pV3D3}\) of 7.8, 15.4, and 22.2 nm.
- **d)** Cumulative distribution of \(C_i\) with \(d_{pV3D3}\) of 7.8, 15.4, and 22.2 nm.
- **e)** Cumulative distribution of \(J_i\) at ±3 MV/cm and **f)** the corresponding \(J_i-E_i\) curves of TaN/pV3D3/Au devices with \(d_{pV3D3}\) of 7.8 nm. The size of the MIM devices is 6.2×10\(^{-4}\) cm\(^2\), and for cumulative distribution, at least 20 MIM devices were randomly selected over an area of 5×5 cm\(^2\). All the measurement was performed in an air environment.

The observations are fully consistent with Al/pV3D3/Al MIM devices in Figure 2 and S6.

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Metallic TaN electrodes are widely adopted as gate electrodes in modern CMOS technologies for use with ultrathin dielectrics (including those with thickness smaller than 5-10 nm) due to their excellent stability. Together with the inertness of Au electrode, the superior chemical and thermal stability of TaN electrode enables critical testing of ultrathin dielectrics while suppressing the chance of accidental oxide formation. For more details on TaN electrodes, please refer to Refs. 21-23.
**Part B. Characteristics of Au/pV3D3/Au devices.**

**a)** Cross-sectional TEM image of an Au/pV3D3 (9.1nm)/Au device. Inset image indicates the MIM device structure. **b)** Cumulative plot of the capacitance per unit area ($C_i$). **c)** Cumulative plot of the leakage current density ($J_i$) at ±3 MV/cm. **d)** Plot for $J_i$ vs. applied field ($E_i$) of the Au/pV3D3 (9.1nm)/Au device.

The cross-sectional TEM image of an Au/pV3D3/Au device shown in Part B-a clearly indicates the formation of sub-10nm-thick pV3D3 layers with the thickness of 8.4±1.1 nm, in reasonable agreement with the macroscopic thickness estimated by the capacitance measurement (= 9.1 nm; **Figure S7 Part B-b**). As can be seen in Part B-c and d, five MIM devices exhibit $J_i$ below approx. $10^{-7}$ A/cm² at the applied field ($E_i$) at 3 MV/cm, indicating that the insulating property of ultrathin pV3D3 layers is also excellent even with Au electrodes.
Part C. Device yield of Au/pV3D3/Au devices. a) The device structure (left) and the cross-sectional TEM image (right) of an Au/pV3D3 (12 nm)/Au device. Electrical characteristics of b) Au/pV3D3 (12 nm)/Au devices and c) Au/pV3D3 (13.4 nm)/Au devices: Cumulative plot of the capacitance per unit area (C) (left); cumulative plot of the leakage current density (J) at ±3 MV/cm (middle); and the plot for J vs. applied field (E) (right).

As can be seen in the plot shown in Part B-d, the device yield related to \( J_i \) appears to be not as great as those of the pV3D3 MIM devices with Al or TaN electrodes (See Figure S6 and S7 Part A). Out of the 14 Au/pV3D3 (9.1 nm)/Au devices tested\(^8\), 13 devices exhibited \( J_i (E_i = 3 \, \text{MV/cm}) \) on the order of \( 10^{-4} \, \text{A/cm}^2 \) or less, and one device exhibited a complete failure; only 7 (5) out of those 14 devices [50% (36%)] exhibited \( J_i (E_i = 3 \, \text{MV/cm}) \) of low \( 10^{-6} \, \text{A/cm}^2 \) (10\(^{-7} \, \text{A/cm}^2 \)) or less.

While even the present results may still be regarded reasonably good for ultrathin polymer dielectrics especially considering that these devices were fabricated in a non-clean-room lab environment, the relatively low yield of Au-based devices seems to stem from the local thickness non-uniformity associated with the rough surface topography of Au electrodes; one may note the nanometric features with the vertical and horizontal characteristic dimensions of 2-3 nm and 10-20 nm, respectively, in the bottom Au electrodes shown in the cross-sectional TEM images (Part B-a). It turns out that the device yield substantially improves even with a small incremental increase in the thickness of a pV3D3 layer as shown in Part C; with the 12nm-thick pV3D3 layer (see the cross-sectional TEM image in Part C-a, for example, 13 out of 16 Au/pV3D3/Au devices (81%) showed \( J_i (E_i = 3 \, \text{MV/cm}) \) on the order of low \( 10^{-8} \, \text{A/cm}^2 \) or less; with the 13.5nm-thick pV3D3 layer, 14 out of 16 devices (87.5%) exhibited a similar or better level of leakage characteristics.

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\(^8\) There were 16 devices in total; two devices were excluded due to accidental scratches made during handling.
Figure S8.

Time-dependent dielectric breakdown characteristics of the 6 nm-thick pV3D3 layer using Al/pV3D3/Al devices. 

- **a)** Evolution of stress current density ($J_{\text{stress}}$) under constant voltage stress where the voltage is ramped from the value corresponding to stress electric field ($E_{\text{stress}}$) of 4 MV/cm to that corresponding to 6.5 MV/cm by 0.5 MV/cm with stress duration of 100 sec for each step. 
- **b)** Evolution of $J_{\text{stress}}$ with $E_{\text{stress}}$ of 5.5 MV/cm for 3 ksec. 
- **c)** $J_{\text{stress}}-E_i$ curves measured before and after the $E_{\text{stress}}$ of 5.5 MV/cm for 3 ksec and 30 ksec. 
- **d)** Evolution of $J_{\text{stress}}$ with $E_{\text{stress}}$ of 4 MV/cm for 3.9 ksec. 
- **e)** $J_{\text{stress}}-E_i$ curves measured before and after the $E_{\text{stress}}$ of 4 MV/cm for 3 ksec and 39 ksec.

From voltage ramp stress test, it is verified that 6 nm-thick pV3D3 layers show a soft breakdown behavior at $E_{\text{stress}}$ in between 5.5 MV/cm and 6 MV/cm (**Figure S8a**). In a long-term time dependent dielectric breakdown (TDDB) test with $E_{\text{stress}}$ of 5.5 MV/cm, the 6 nm-thick pV3D3 layers showed soft breakdown for the stress time over 500 sec (**Figure S8b**). And $J_i$ slightly increased by a prolonged stress of 30 ksec, but it was still significantly low without catastrophic failure (**Figure S8c**). In fact, the device remained intact with a relatively high stress field of 4 MV/cm for 39 ksec (**Figure S8d** and **e**).
Figure S9. X-ray reflectivity (XRR) spectra of pV3D3 thin films with various thickness ($d_{pV3D3}$). a) XRR data and corresponding fits as a function of 2-theta (left) and $q_z$ (right). Inset figure indicates the sample structure used for the analysis. b) Bulk density and surface roughness of pV3D3 as a function of $d_{pV3D3}$. All values were obtained from the XRR data in a).

X-ray reflectivity (XRR) measurement of pV3D3 layer was performed with various $d_{pV3D3}$ from ca. 7.5 to 21 nm. In the XRR spectra, all pV3D3 samples exhibited the classical Kießig fringe behavior, and the simulational fits were well overlapped with the experimental data set. From this fitting data, the thickness, bulk density, and surface roughness of pV3D3 films could be extracted (The detailed experimental and analytical procedures were described in the previous literatures.9,10). The thicknesses measured from the XRR results are matched very well to the $d_{pV3D3}$ determined by ellipsometry method (data not shown). The bulk density of pV3D3 was 1.704 ± 0.021 g/cm$^3$ which is higher than that of most of organosilicone polymers such as polydimethylsiloxane (PDMS, 0.965 g/cm$^3$) and poly(phenylsilsesquioxane) (1.56 g/cm$^3$), indicating that the pV3D3 layer is densely packed due to the high degree of the crosslinking sites, in spite of its amorphous nature. The density values were uniform with various $d_{pV3D3}$, which strongly infers that the iCVD process could form a uniform films even for ultra-low range of $d_{pV3D3}$ below 10 nm and does not form “interfacial layer” on the SiO$_2$ layer, which is well consistent with the excellent down-scalability of pV3D3 insulating layers even below 10 nm. The surface roughness value obtained from XRR was 0.373 ± 0.043 nm in root-mean-square, and also well consistent with the results from atomic force microscopy (AFM) analysis in Table S2.

Figure S9.

X-ray reflectivity (XRR) spectra of pV3D3 thin films with various thickness ($d_{pV3D3}$). a) XRR data and corresponding fits as a function of 2-theta (left) and $q_z$ (right). Inset figure indicates the sample structure used for the analysis. b) Bulk density and surface roughness of pV3D3 as a function of $d_{pV3D3}$. All values were obtained from the XRR data in a).

X-ray reflectivity (XRR) measurement of pV3D3 layer was performed with various $d_{pV3D3}$ from ca. 7.5 to 21 nm. In the XRR spectra, all pV3D3 samples exhibited the classical Kiessig fringe behavior, and the simulational fits were well overlapped with the experimental data set. From this fitting data, the thickness, bulk density, and surface roughness of pV3D3 films could be extracted (The detailed experimental and analytical procedures were described in the previous literatures.\(^9\,\,10\)). The thicknesses measured from the XRR results are matched very well to the $d_{pV3D3}$ determined by ellipsometry method (data not shown). The bulk density of pV3D3 was $1.704 \pm 0.021$ g/cm$^3$ which is higher than that of most of organosilocone polymers such as polydimethylsiloxane (PDMS, 0.965 g/cm$^3$) and poly(phenylsilsesquioxane) (1.56 g/cm$^3$), indicating that the pV3D3 layer is densely packed due to the high degree of the crosslinking sites, in spite of its amorphous nature. The density values were uniform with various $d_{pV3D3}$, which strongly infers that the iCVD process could form a uniform films even for ultra-low range of $d_{pV3D3}$ below 10 nm and does not form “interfacial layer” on the SiO$_2$ layer, which is well consistent with the excellent down-scalability of pV3D3 insulating layers even below 10 nm. The surface roughness value obtained from XRR was $0.373 \pm 0.043$ nm in root-mean-square, and also well consistent with the results from atomic force microscopy (AFM) analysis in Table S2.


Figure S10.

Evolution of simplified energy band structure according to the applied voltage and its relation to $J_i$-$E_i$ characteristics. 

a) Schematic energy band diagram of Al/pV3D3/Al devices at four different regions of $V_i$ that gradually increases from 0 to a voltage larger than $q\Phi_b$, where $q$ and $\Phi_b$ represent the electronic charge and barrier height, respectively. 

b) A $J_i$-$E_i$ curve of the MIM device with a 6 nm-thick pV3D3 layer with the representative voltage ranges.

The energy diagrams shown in Figure S10a illustrate well that a tunneling conduction through the pV3D3 layer is governed by direct tunneling for $0 < V_i < q\Phi_b$ and that it is governed by Fowler-Nordheim (F-N) tunneling for $V_i > q\Phi_b$. Such a transitional behavior can be easily observed in Figure S10b.\(^{11}\)

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Evolution of simplified energy band structure according to the applied voltage and its relation to $V_g$ governed by direct tunneling for $0 < V_g$ the MIM device with a 6 nm-thick pV3D3 layer with the representative voltage ranges.

Table S4.

Characteristic parameters of C$_{60}$ FETs with pV3D3 GIs of various thicknesses.

<table>
<thead>
<tr>
<th>$L \times W^a$</th>
<th>$C_i^b$ [nF/cm$^2$]</th>
<th>$d_{pV3D3}$ [nm]</th>
<th>$\mu_{FET}$ $^c$ [cm$^2$/Vs]</th>
<th>$V_T$ $^c$ [V]</th>
<th>$SS^c$ [V/decade]</th>
<th>on-off$^c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>200×1000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>45.3</td>
<td>42.9</td>
<td>1.53±0.08</td>
<td>2.86±0.018</td>
<td>462m±9m</td>
<td>$&gt;10^4$</td>
</tr>
<tr>
<td></td>
<td>89.9</td>
<td>21.6</td>
<td>1.49±0.09</td>
<td>1.09±0.025</td>
<td>256m±16m</td>
<td>$&gt;10^5$</td>
</tr>
<tr>
<td></td>
<td>127</td>
<td>15.3</td>
<td>1.32±0.06</td>
<td>0.64±0.010</td>
<td>173m±4m</td>
<td>$&gt;10^5$</td>
</tr>
<tr>
<td></td>
<td>159</td>
<td>12.2</td>
<td>0.993±0.056</td>
<td>0.51±0.022</td>
<td>138m±14m</td>
<td>$&gt;10^5$</td>
</tr>
</tbody>
</table>

$^a L$ and $W$ represent channel length and width, respectively.
$^b C_i$ was measured at 1 kHz.
$^c$ Average and standard deviation values were extracted from 5 different FETs for each case.

C$_{60}$ FETs with various thicknesses of pV3D3 GIs show outstanding device characteristics with low gate leakage current ($I_G$), field-effect mobility ($\mu_{FET}$) of c.a. 1.5 cm$^2$/Vs, on-off ratio over $10^5$, and negligible hysteresis. The threshold voltage ($V_T$) and subthreshold swing ($SS$) decreased as the $d_{pV3D3}$ decreased, and reached 0.51 and 138 mV/decade, respectively, with the $d_{pV3D3}$ of 12.2 nm corresponding to a $C_i$ of 159 nF/cm$^2$. Low $I_G$ was maintained for $d_{pV3D3}$ down to 12.2 nm, but a slight decrease of $\mu_{FET}$ was also observed from the devices with $d_{pV3D3}$ under ~15 nm.
Figure S12.

Roughness of each gate electrodes shown in Figure 3c and Table 1. AFM images of Al (left), indium tin oxide (ITO) (middle), and Ag-ink (right) electrodes. The roughness of each electrode varied with respect to the material. In particular, the Ag-ink electrode was extremely rough with a RMS roughness of almost 20 nm.
Figure S12.

Roughness of each gate electrodes shown in Figure 3c and Table 1. AFM images of Al (left), indium tin oxide (ITO) (middle), and Ag-ink (right) electrodes. The roughness of each electrode varied with respect to the material. In particular, the Ag-ink electrode was extremely rough with a RMS roughness of almost 20 nm.

Figure S13.

Bottom-gated C₆₀ FETs with pV3D3 GIs on various substrate materials, including glass, polyethylene terephthalate (PET), and cellophane tape. a) Transfer and b) output characteristics of bottom-gated C₆₀ FETs with pV3D3 GIs on various substrate materials, including glass, PET, and cellophane tape.

Table S5.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass</td>
<td>200×1000</td>
<td>51.3</td>
<td>38.0</td>
<td>0.961</td>
<td>2.73</td>
<td>0.518</td>
<td>&gt;10⁵</td>
</tr>
<tr>
<td>PET</td>
<td>51.3</td>
<td>38.0</td>
<td>0.961</td>
<td>2.73</td>
<td>0.518</td>
<td>&gt;10⁵</td>
<td></td>
</tr>
<tr>
<td>Cell.-tape</td>
<td>45.4</td>
<td>42.9</td>
<td>1.204</td>
<td>2.026</td>
<td>0.506</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

As can be seen Figure S13, the FET performance of bottom-gated C₆₀ FETs was not impacted significantly by the change in the substrate materials. Even with highly vulnerable substrates such as PET and cellophane tape, the μ_FET was greater than 0.5 cm²/Vs, and the on-off ratio was higher than 10⁵. Note that no pretreatment including flattening of the surface of PET and cellophane tape was applied. The highly reliable FET performance can be ascribed to the damage-free deposition of pV3D3 layers on various substrates via iCVD.
Figure S14.

Top-gated P3HT FETs with solution processed poly(methyl methacrylate) (PMMA) and iCVD pV3D3 as GIs. a) Schematic structure of top-gated P3HT FETs. b) Chemical structures of P3HT and PMMA, and c) the transfer (top) and output (bottom) characteristics of top-gated P3HT FETs with 500 nm-thick PMMA GIs, and 171 nm and 17.2 nm-thick pV3D3 GIs. 12,13 d) The change of $I_D$ normalized to its initial value during constant voltage stress test in the “diode connection” at a stress bias ($V_{G,str}$) of -12 V for 3,000 sec. e) The transfer characteristics of top-gated P3HT FETs with 38 nm-thick pV3D3 GI before and after the constant voltage stress.

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Figure S14. Top-gated P3HT FETs with solution processed poly (methyl methacrylate) (PMMA) and iCVD pV3D3 as GIs.

a) Schematic structure of top-gated P3HT FETs, b) chemical structures of P3HT and PMMA, and c) the transfer (top) and output (bottom) characteristics of top-gated P3HT FETs with 500 nm-thick PMMA GIs, and 171 nm and 17.2 nm-thick pV3D3 GIs. 12,13 d) The change of $I_D$ normalized to its initial value during constant voltage stress test in the “diode connection” at a stress bias ($V_{G,str}$) of -12 V for 3,000 sec. e) The transfer characteristics of top-gated P3HT FETs with 38 nm-thick pV3D3 GI before and after the constant voltage stress.

Table S6.

<table>
<thead>
<tr>
<th>Dielectrics</th>
<th>$L \times W$ [μm×μm]</th>
<th>$C_i^a$ [nF/cm²]</th>
<th>$d_i^c$ [nm]</th>
<th>$\mu_{FET}$ [cm²/Vs]</th>
<th>$V_T$ [V]</th>
<th>on-off [–]</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMMA</td>
<td>50×1000</td>
<td>6.2$^a$</td>
<td>500</td>
<td>0.051</td>
<td>20.0</td>
<td>$&gt;10^3$</td>
</tr>
<tr>
<td>pV3D3</td>
<td></td>
<td>11.4$^b$</td>
<td>171</td>
<td>0.066</td>
<td>12.6</td>
<td>$&gt;10^3$</td>
</tr>
<tr>
<td>pV3D3</td>
<td></td>
<td>54.1$^b$</td>
<td>36.0</td>
<td>0.060</td>
<td>2.8</td>
<td>$\sim 10^3$</td>
</tr>
<tr>
<td>pV3D3</td>
<td></td>
<td>113$^b$</td>
<td>17.2</td>
<td>0.062</td>
<td>1.8</td>
<td>$\sim 10^4$</td>
</tr>
</tbody>
</table>

$^a$ $C_i$ of PMMA GIs was calculated from the thickness of 500 nm and $k_{PMMA}$ of 3.5.

$^b$ $C_i$’s of pV3D3 GIs were measured from MIM devices on separate substrates that were fabricated in the same batch with the FETs.

$^c$ $d_i$ represents the thickness of the dielectric layer, PMMA or pV3D3.

Top-gated P3HT FETs with pV3D3 GIs showed comparable channel characteristics to the reference device with PMMA GIs. The top-gated P3HT FETs with 17.2 nm-thick GIs showed low-voltage operation switchable under 3 V with low gate leakage current and homogeneous channel characteristics together with the device with thick pV3D3 GIs. The top-gated P3HT FETs showed an outstanding stability against a constant voltage stress as long as 3,000 s and higher than 90% of initial $I_D$ was retained after the constant voltage stress. The transfer characteristics after the constant voltage stress also clearly indicates that the fabricated top-gated P3HT FETs are highly electrically stable.
Figure S15.

Surface morphologies of iCVD processed pV3D3 layers deposited on graphene. a) RMS surface roughness ($R_q$) of graphene and pV3D3 layers deposited on SiO$_2$ and graphene. b) Surface morphologies of graphene and pV3D3 layers deposited on graphene.
Figure S16.

Top-gated graphene FETs with atomic layer deposited (ALD) Al$_2$O$_3$ and iCVD pV3D3 as GIs. a) An optical microscope image of a top-gated graphene FET. b) Output characteristics of top-gated graphene FETs with 7.8 nm-thick pV3D3 GIs. c) Transfer characteristics of top-gated graphene FET with 25 nm-thick ALD Al$_2$O$_3$ GI at $V_D = 1$ V.

The $\mu_{\text{FET}}$ of a graphene FET was extracted using the following equation:\textsuperscript{14}

$$
\mu_{\text{FET}} = \frac{L G_m}{W C V_D}
$$

where $G_m$ is the two-terminal transconductance ($G_m = dI_D/dV_G$). Considering that the two-terminal $G_m$ includes a graphene/metal contact resistance, the intrinsic mobility of the graphene channels is likely higher than the calculated values shown in Table 2. As a control, a top-gated graphene FET with ALD Al$_2$O$_3$ GI was also fabricated and the performance of the graphene FET was compared with that of top-gated graphene FET with iCVD pV3D3 GI in Table 2.

Figure S17.

Electrical characteristics of Al/AlO\textsubscript{x} (5 nm)/Al devices vs. Al/pV3D3 (5.9 nm)/Al devices.

To minimize the chance of native oxide formation in Al-containing devices as much as possible, devices for electrical measurement were kept within the inert environment throughout device fabrication and measurement. Even if one may not completely exclude the chance of forming the trace amount of oxides at the interfaces, its electrical effect should be insignificant for such environmentally-controlled devices. To check this notion further, we had electrically tested the insulating performance of Al/AlO\textsubscript{x} (5 nm)/Al in which AlO\textsubscript{x} was intentionally formed by applying an oxygen plasma on top of the bottom Al electrode (50 W, 25 sccm of O\textsubscript{2} for 5 min). The insulating property of this MIM device (Al/AlO\textsubscript{x} (5 nm)/Al) could not reach the level of pV3D3 layers and had leakage current that was much larger than that of Al/pV3D3 (5.9 nm)/Al by several orders of magnitude. Since the insulating performance of accidentally formed oxides should be even far poorer than that of O\textsubscript{2}-plasma-generated AlO\textsubscript{x}, its effect, if any, should be insignificant even with consideration of “hybrid” effect when combined with that of pV3D3.